as concl sub C3 a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

sub B3 6. (Amended) A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for corresponding one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

SUB C4 7. (Amended) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

## REMARKS

The Office Action dated November 7, 2001, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1-7 have been amended. Additionally, the specification has also been amended. A new title, as suggested by the Examiner, and drawing corrections made to Figure 2, are respectfully submitted for consideration. No new matter has been added

by the amendments made herein. Therefore, claims 1-7 are pending in the present application and are respectfully submitted for consideration.

The drawings were objected to because the label "(PROL)" of Figure 2 is mislabeled and should be --(PORL)--. Applicant appreciates the Examiner's courtesy in highlighting this deficiency; attached is a Request for Approval of Drawing Corrections with proposed changes to Figure 2 highlighted in red. Changes to Figure 2 are respectfully submitted for consideration. Upon approval of this request, formal drawings will be timely filed.

The title of the invention was objected to on the grounds that it was not adequately descriptive. The original title has been cancelled and the new title, POWER-ON RESET CIRCUIT/METHOD FOR INITIALIZING AN INTEGRATED CIRCUIT, is respectfully submitted for consideration. The disclosure of the present application was objected to as containing some minor informalities therein. Applicant respectfully submits that the amendments made herein to the disclosure of the present application overcome the minor informalities noted in the Office Action. Accordingly, Applicant respectfully requests that the objection to the disclosure be withdrawn.

Claims 2, 4 and 6 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicant respectfully submits that the amendments made to the claims overcome the rejection noted in the Office Action and place the claims in compliance with U.S. patent practice.

Claims 1-7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Malherbe (U.S. Patent No. 6,252,442 B1). Applicant submits that each of claims 1-7 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Claim 1 recites a semiconductor integrated circuit comprising a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other. The semiconductor integrated circuit also comprises a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit according to at least one from any of the sub power-on reset signals.

Claim 3 recites a semiconductor integrated circuit comprising a sub reset signal generator for generating a sub power-on reset signal, a reset terminal for receiving an external power-on reset signal, and a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of the sub power-on reset signals and the external power-on reset signal.

Claim 5 recites a semiconductor integrated circuit comprising a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other, a reset terminal for receiving an external power-on reset signal, and a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of the sub power-on reset signals and said external power-on reset signal.

Claim 7 recites a method of initializing a semiconductor integrated circuit comprising the steps of generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other, and initializing an internal circuit according to at least one from any of the power-on reset signals.

Accordingly, the essence of the present invention with respect to at least claim 1 is a semiconductor integrated circuit having a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of the sub power-on reset signals. As such, the present invention results in the advantage of initializing internal circuits of a semiconductor by reliably generating a power-on reset signal without depending on the characteristics of a transistor therein.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the presently pending claims, and therefore, fails to provide the advantages which are provided by the present invention.

Malherbe discloses an electronic circuit provided with a neutralization device that is designed to block the operation of any electronic circuit when the device is insufficiently supplied. The neutralization device of Malherbe is designed especially for electronic circuits supplied with low supply voltages. The device comprises an upline with respect to an inhibiting means to block the operation of the electronic circuit, a control circuit reproducing the critical path or the potential critical paths of the functional electronic circuit in the form of elementary circuits. The deactivation of the inhibiting means is done only when the totality of the elementary circuits delivery same-state elementary signals indicating that the supply voltage is sufficient to ensure their efficient operation.

Applicant respectfully submits that each and every element recited within claims 1, 3, 5 and 7 of the present application is neither disclosed nor suggested by Malherbe. In particular, Applicant respectfully submits that the power-on reset circuit and the

method for initializing an integrated circuit as recited in the present application is clearly distinct from that which is illustrated in Malherbe. Specifically, it is submitted that Malherbe fails to disclose or suggest a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other, and a main reset signal generator for generating a pulse signal, which is a main power-on reset signal, to initialize an internal circuit according to at least one from any of the sub power-on reset signals. As mentioned above, Malherbe merely discloses a control circuit that only generates control signals for controlling an inhibiting circuit which controls operations of an electronic circuit, rather than generating pulse signals which are generated by the main reset signal generator of the present invention. In other words, when the states of a plurality of signals (POR 1-PORn) from a plurality of circuits are the same, the invention as disclosed in Malherbe merely outputs the same signal (POR) of that state from the OR circuit. However, the OR circuit in Malherbe does not output pulse signals, and therefore, Applicant respectfully submits that Malherbe fails to disclose or suggest each and every element recited within claims 1, 3, 5 and 7 of the present application.

As for claims 2, 4 and 6, Applicant submits that each of these claims recites subject matter which is neither disclosed nor suggested by the cited prior art. In particular, each of these claims depends on independent claims 1, 3 and 5, respectively. Therefore, each of these claims incorporates each and every limitation recited within claims 1, 3 and 5, respectively therein. Therefore, Applicant submits that each of claims 2, 4 and 6 also recites subject matter which is neither disclosed nor

suggested by Malherbe for at least the reasons set forth above with respect to claims 1, 3 and 5.

Claims 1-3, 5 and 7 were rejected under 35 U.S.C. § 102(e) as being anticipated by Crotty (U.S. Patent No. 6,078,201). Applicant submits that each of claims 1-3, 5 and 7 recites subject matter that is neither disclosed nor suggested in the cited prior art.

Crotty discloses a power-on reset circuit for dual supply voltages. Figure 2 of Crotty illustrates the power-on reset circuit 200, which includes a dual-voltage detection circuit 210 coupled to a first supply voltage terminal Vcc1, a second supply voltage terminal Vcc2, and a ground terminal. The dual-voltage detection circuit 210 determines whether supply voltage Vcc1 is greater than a first adequate voltage level Vad1 and in response outputs a first voltage detection signal VD1. Circuitry coupled to second supply voltage terminal Vcc2 drives first voltage detection signal VD1 on output terminal 211. If first supply voltage Vcc1 is less than the first adequate voltage Vad1, the dual-voltage detection circuit 210 drives first voltage detection signal VD1 to a power-off logic level. If the first supply voltage Vcc1 is greater than the first adequate voltage Vad1, the dual-voltage detection circuit 210 drives the first voltage detection signal VD1 to a power-on logic level.

Applicant respectfully submits that each and every element recited within claims 1, 3, 5 and 7 of the present application is neither disclosed nor suggested by Crotty. In particular, Applicant respectfully submits that the power-on reset circuit and the method for initializing an integrated circuit as recited in the present application is clearly distinct from that which is illustrated in Crotty. Specifically, it is submitted that Crotty fails to disclose or suggest a main reset signal generator for generating a pulse signal as a

main power-on reset signal to initialize an internal circuit, according to at least one from any one of the sub power-on reset signals. Although Crotty discloses a power-on reset circuit, Applicant submits that the power-on reset circuit of Crotty is distinguishable from the present invention because the power-on reset circuit of Crotty comprises two voltage detection circuits, two low pass filters, and a buffer circuit. More importantly, the power-on reset circuit of Crotty does not generate pulse signals as the main reset signal generator does in the present invention. In other words, the power-on reset circuit in Crotty is only for detecting noise from the voltage (VD1 and VD2) from the power detection circuits, rather than having the function of outputting pulse signals as claimed in the present invention. Accordingly, Applicant respectfully submits that Crotty fails to disclose or suggest each and every element recited within claims 1, 3, 5 and 7 of the present application.

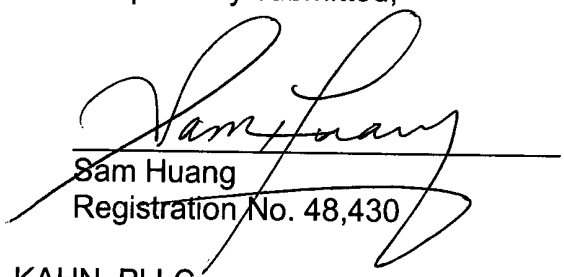
As for claim 2, Applicant submits that claim 2 recites subject matter which is neither disclosed nor suggested by the cited prior art. In particular, claim 2 depends on independent claim 1, and therefore, incorporates each and every limitation recited within claim 1 therein. Therefore, Applicant submits that claim 2 also recites subject matter which is neither disclosed nor suggested by Crotty for at least the reasons set forth above with respect to claim 1.

In view of the above, Applicant respectfully submits that claims 1-7 each recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant also submits that this subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore, respectfully requests that claims 1-7 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully submitted that the Examiner contact by telephone the Applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,



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Enclosure: Request for Approval of Drawing Corrections
Marked-Up Version of Original Paragraphs in the Specification
Marked-up Version of Original Claims

## MARKED-UP VERSION OF ORIGINAL PARAGRAPHS IN THE SPECIFICATION

Please replace the last full paragraph starting with "Recently," on page 1 with:

Recently, the transistor structure of the semiconductor integrated circuit has been further refined. Since the channel length of a transistor is [shorted] shortened, the fluctuation width of the threshold voltage of the transistor is increased due to a short channel effect. The threshold voltage of the transistor varies, depending on the manufacturing conditions of the semiconductor integrated circuit, the chip position on the wafer, and the wafer position of production lots. If the fluctuation width of the threshold voltage is increased, deviation of inactivation timings of the power-on reset signal is also increased.

Please replace the paragraph staring on line 26, page 4 with:

Fig. 5 is a block diagram showing a power-on resetting circuit in a [second] third embodiment of the semiconductor integrated circuit in the present invention.

Please replace the last full paragraph starting on line 25, page 9 with:

The power-on resetting circuit is provided with two sub reset signal generators 10 and 12 and a main reset signal generator 36. The main reset signal generator 36 has pulse generators 16 and 18 respectively corresponding to the sub reset signal generators 10 and 12, a pulse generator 38 that receives a power-on reset signal PORE from the exterior of the power-on resetting circuit, and a composite circuit 40 that receives outputs of the pulse generators 16, 18 and [36] 38.

Please replace the paragraph starting on line 33, page 9 with:

The sub reset signal generators 10 and 12 and pulse generators 16 and 18 are the same as those of the first embodiment. The pulse generator [36] 38 is the same as the pulse generator 16. The composite circuit 40 is constructed of a negative logic OR circuit. The composite circuit 40 receives pulses PLSH, PLSL and PLSE and generates a power-on reset signal POR.

## MARKED-UP VERSION OF ORIGINAL CLAIMS

1. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

2. (Amended) A semiconductor integrated circuit according to claim 1, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating [a pulse in synchronization with] pulses on the basis of a transition edge for [each of] corresponding one of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

3. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.

4. (Amended) A semiconductor integrated circuit according to claim 3, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating [a pulse in synchronization with] pulses on the basis of a transition edge for [each of] corresponding one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

5. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

6. (Amended) A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating [a pulse in synchronization with] pulses on the basis of a transition edge for [each of] corresponding one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

7. (Amended) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of pulse signals as power-on reset signals according to a plurality of sub power-on reset signals at timings different from each other; and

initializing an internal circuit according to at least one from any of said power-on reset signals.

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